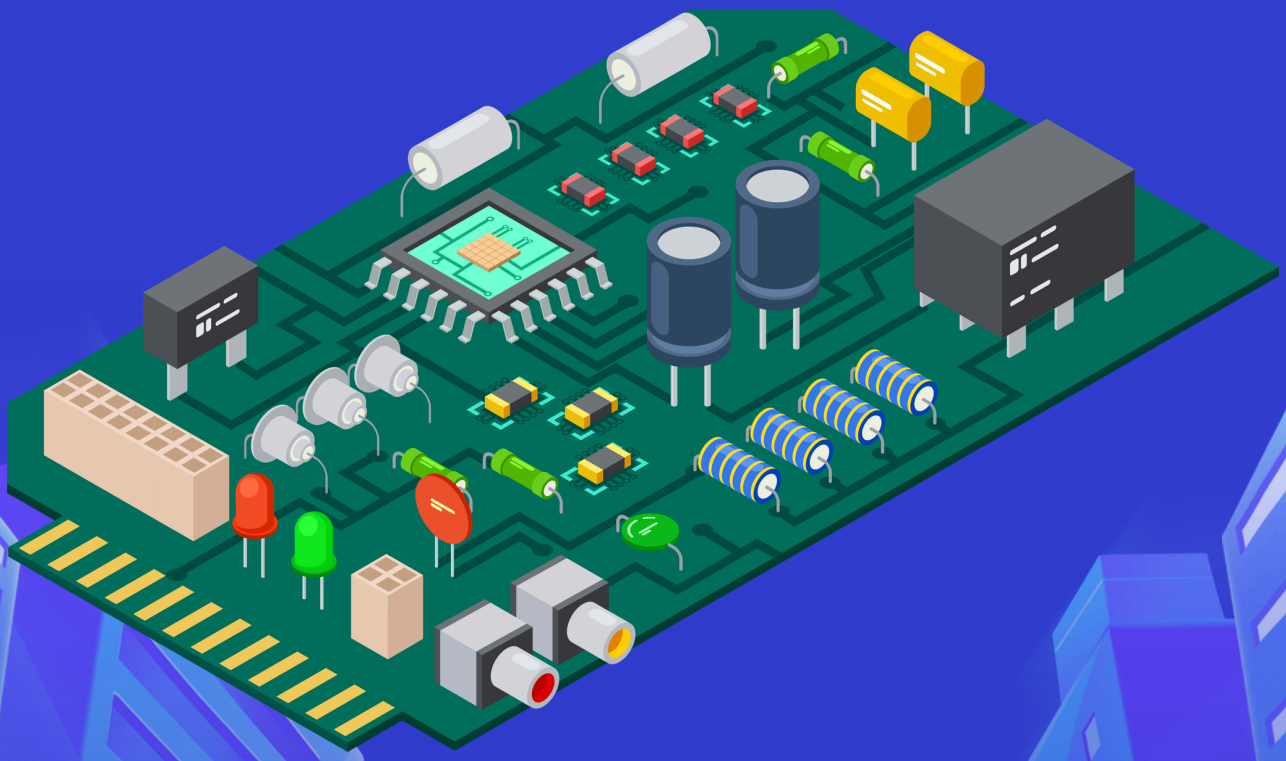
PANTECH SOLUTIONS®
Technology Beyond The Dreams

Pantech e Learning
DIGITAL LEARNING SIMPLIFIED

ASIC RTL DESIGN & VERIFICATION PROFESSIONAL TRACK

Master Digital Logic, RTL Design, SystemVerilog, UVM, and ASIC Verification workflows. Design synthesizable RTL



DESIGN SYNTHESIZABLE RTL, BUILD REUSABLE VERIFICATION ENVIRONMENTS, AND DEVELOP INDUSTRY-READY VLSI VERIFICATION SKILLS USING MODERN EDA TOOLS.

PROFESSIONAL PROGRAM · 6 MONTHS

ASIC RTL DESIGN & VERIFICATION PROFESSIONAL TRACK

Design synthesizable RTL, build reusable verification environments, and develop industry-ready VLSI verification skills using modern EDA tools.

DURATION:
6 MONTHS • 10+ LAB HOURS

FORMAT & MODE
HYBRID LMS + LIVE

SKILL LEVEL
GRADUATE / PROFESSIONAL

ASIC RTL DESIGN & VERIFICATION SPECIALIZATION TRACKS

Master the complete VLSI Design and Verification flow through four industry-focused specialization.

Track 01
Digital Logic & VLSI Fundamentals

Learn digital electronics, Boolean algebra, FSM design, timing analysis, and ASIC design fundamentals.

- Digital Logic Design
- Sequential Circuits
- Finite State Machines

Track 02
Verilog RTL Design

Develop synthesizable RTL using Verilog, simulation techniques, timing controls, and memory modeling.

- RTL Coding
- Simulation & Timing
- Memory & Interfaces

Track 03
SystemVerilog Verification

Build advanced verification environments using OOP, assertions, constrained random testing, and functional coverage.

- Assertions (SVA)
- Coverage Analysis
- Random Verification

Track 04
UVM & Protocol Verification

Develop reusable UVM environments, protocol VIPs, scoreboards, agents, and regression frameworks..

- UVM Testbenches
- AXI/APB Verification
- Coverage & Regression

INDUSTRY-GRADE TOOLCHAIN YOU'LL MASTER

'VERILOG', 'SYSTEMVERILOG', 'UVM', 'MODELSIM', 'QUESTA', 'VCS', 'XCELIUM', 'VIVADO', 'SYNOPSYS', 'AXI', 'AHB', 'APB', 'AMBA', 'SVA', 'DPI-C', 'GIT', 'CI FOR RTL', 'WAVEFORM VIEWER', 'COVERAGE ANALYSIS', 'FORMAL VERIFICATION'

TRACK 01
DIGITAL LOGIC & VLSI FUNDAMENTALS

Digital Logic Fundamentals
- checkBoolean Algebra
- checkLogic Gates
- checkKarnaugh Maps

Combinational Logic Design
- checkMultiplexers Demultiplexers
- checkEncoders & Decoders
- checkArithmetic Circuits

Sequential Logic
- checkFlip-Flops & Latches
- checkCounters & Registers
- checkTiming Analysis

Finite State Machines
- checkMealy & Moore FSM
- checkState Encoding
- checkState Minimization

Capstone Milestone 1: Digital System Design and Simulation

Design and simulate a digital system using combinational logic, sequential circuits, and finite state machines.

TRACK 02
VERILOG RTL DESIGN

Verilog Basics
- checkModules
- checkPorts
- checkData Types

RTL Coding
- checkBehavioral Modeling
- checkDataflow Modeling
- checkGate-Level Modeling

Timing & Simulation
- checkalways Blocks
- checkBlocking vs Non-Blocking
- checkSimulation Events

Memory & Interfaces
- checkRAM
- checkROM
- checkFIFO
- checkUART/SPI RTL

Capstone Milestone: Synthesizable Verilog RTL Design Suite

Design an ALU, UART Controller, FIFO, and Memory Controller using synthesizable Verilog RTL.

TRACK 03
SYSTEMVERILOG VERIFICATION

SystemVerilog Features
- checkInterfaces
- checkPacked Arrays
- checkClocking Blocks

OOP Testbench
- checkClasses
- checkInheritance
- checkVirtual Interfaces

Assertions & Randomization
- checkSVA
- checkConstrained Random
- checkFunctional Coverage

Debug & Coverage
- checkCoverage Closure
- checkDPI-C
- checkPackages

Capstone Milestone: Reusable SystemVerilog Verification Environment

Develop reusable SystemVerilog verification environments with assertions and functional coverage.

TRACK 04
UVM & PROTOCOL VERIFICATION

UVM Fundamentals
- checkFactory
- checkPhasing
- checkConfiguration DB

UVM Components
- checkDriver
- checkMonitor
- checkAgent
- checkScoreboard

Sequences
- checkSequencers
- checkVirtual Sequences
- checkTransaction-Level Modeling

Protocol Verification
- checkAXI
- checkAPB
- checkAHB
- checkRegister Models

Capstone Milestone: Complete UVM Verification Environment

Build a complete UVM Verification Environment for an AXI/APB peripheral including agents, scoreboards, assertions, coverage, and regression testing.

BRIDGE THE GAP FROM LEARNING EV CONCEPTS TO INDUSTRY-READY ELECTRIC VEHICLE ENGINEER

Transform from understanding EV fundamentals to designing, simulating, controlling, and building real Electric Vehicle systems with industry-standard tools and hardware.

WHERE YOU START

01 | Basic Digital Electronics Knowledge
Limited exposure to digital logic, HDL programming, and semiconductor workflows..

02 | No RTL Design Experience
No practical experience writing synthesizable Verilog or FPGA-ready RTL.

03 | No Verification Knowledge
Limited understanding of SystemVerilog, assertions, coverage, or UVM methodology.

WHERE YOU'LL BE

RTL Design Engineer
Design synthesizable Verilog RTL for FPGA and ASIC applications.

Verification Engineer
Build reusable SystemVerilog and UVM verification environments

Industry-Ready EV Portfolio
Complete multiple RTL Design, FPGA, SystemVerilog, and UVM projects ready for semiconductor interviews.

READY TO MAKE THIS TRANSFORMATION ?
JOIN 2,400+ ENGINEERS WHO ALREADY MADE THE LEAP.

INSIGHTS FROM OUR INTERNS

TRUSTED BY 8,880+ ON GOOGLE

From Graduate to FPGA Engineer

"The Verilog and FPGA implementation modules gave me the confidence to work on real hardware projects."

KARTHIK R

RTL Design Made Simple

"The hands-on RTL coding sessions and simulation labs prepared me for real semiconductor projects."

SHREYA P.

Mastered UVM in 12 Weeks

"The SystemVerilog and UVM labs helped me confidently develop reusable verification environments."

ROHIT V.

Embedded to ASIC

"I transitioned from Embedded Systems to ASIC Verification and landed my dream semiconductor job."

PRIYANKA G.

FPGA Projects Opened Doors

"The FPGA implementation projects became the strongest part of my interview portfolio."

SNEHA A.

ECE Graduate to Verification Engineer

"The practical UVM projects helped me secure my first role as a Verification Engineer."

NIKHIL M.

HYBRID TRAINING EXPERIENCE

Seamlessly blend online theoretical depth with offline real-world practicals. Gain hands-on exposure to industrial hardware, live projects, and internship opportunities.

ONLINE + OFFLINE LABS
LIVE SESSIONS PAIRED WITH IN-LAB CODING PRACTICALS. TERMINAL

WORK ON FPGA BOARDS AND LIVE ASIC/RTL PROJECTS.

INTERNSHIP OPPORTUNITIES
APPLY YOUR SKILLS WITH AI ENGINEERING TEAMS.

EARN PRESTIGIOUS VERIFIABLE CREDENTIALS

Your certification formally validates your skill set in recruiter searches.

VERIFIABLE CREDENTIALS TOKEN

Unique cryptographic hashes registered on global validation boards.

PREMIUM LINKEDIN INTEGRATIONS

Add directly to your credentials panel with pre-filled ID tracking.

PROGRAM INVESTMENT

Live Masterclasses & Q&A
Industry Expert Instructors
Practical Case Studies

- 6 MONTHS
- 240+ LAB HOURS
- Flexible 0% EMI Options

Master Digital Logic, Verilog HDL, SystemVerilog, FPGA Design, ASIC Design Flow, and UVM Verification through industry-focused projects. Enroll in the next batch and build a **portfolio that semiconductor recruiters value**.

INR 8474 +GST

TOTAL INR 59,999* (INCLUSIVE OF TAXES)

READY TO BECOME AN INDUSTRY-READY RTL DESIGN ENGINEER?

CONTACT US

SRINIVASAN N 98409 74407

KUMARASAMY R 95661 33338